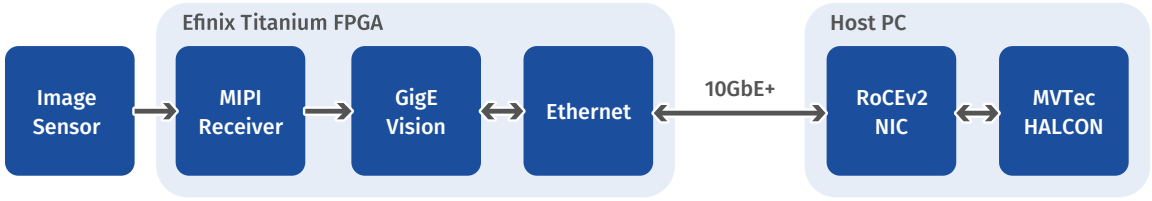
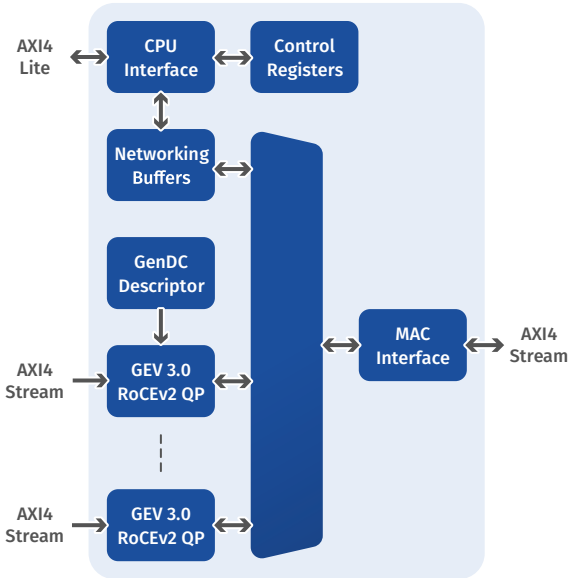
GigE Vision 3.0 RoCEv2 Device for Efinix Titanium FPGAs

Overview

- Reference implementation of a GigE Vision 3.0 device
- Built around the imavix engineering GigE Vision IP core
- Implemented in the Efinix Titanium power-efficient FPGA
- Hardware-offloaded RoCEv2-based GVRSP streaming protocol
  - High performance – Low latency – High efficiency – Reliability – Data consistency
- GenICam GenDC universal payload data type
- Software control implemented in the RISC-V SoC
- MVTec HALCON as the host software





GigE Vision 3.0 IP Core

- GigE Vision 3.0 stream transmitter
- Native support of the GenICam GenDC payload type
- RoCEv2-based GVRSP streaming protocol implemented in the FPGA fabric
- Fully customizable core configuration
- Supported data rates up to 100 Gb/s
- Accompanied by a basic embedded software
- Targets Efinix power-efficient FPGAs

About imavix engineering

- FPGA IP cores with related development and consultancy services
- Image sensor and camera interfacing
- PCIe host interfaces with DMA streaming engines
- GenICam based standard machine vision interfaces
- Ethernet and GigE Vision transport layers including the RDMA/RoCEv2 technology

imavix engineering s.r.o.
Cholunná 17, 394 68 Žirovnice
Czech Republic

www.imavix.com
E: info@imavix.com
T: +420 723 760 802